A review on Buck topology-based PFC Conversion Techniques

[1]Ahmar Farooque Dahri [2]Anwar Ali Sahito, [3]Abdul Hakeem Memon, [4]Shahzor Ahmed Memon
[1, 4] Student M.E. (Electrical Power), [2] Associate Professor, [3] Assistant Professor
[1, 4] Institute of Information and Communication Technologies, [2, 3,] Department of Electrical Engineering,
Mehran University of Engineering & Technology, Jamshoro, Pakistan
Email – [1]Dahri.ahmar@outlook.com

Abstract: *During the last few decades, power factor correction (PFC) converters has been a subject of great importance because of its wide usage and various applications like switch mode power supplies (SMPS), Adjustable speed drives, etc. Majorly, boost PFC converters have been widely utilized because of its inherent current shaping ability, although the output of boost converter is usually more than the input and to achieve high gain a relatively large duty cycle is required and thermal concern also limits the power density increase at low line input. These demerits at low line input can be overcome by utilizing a buck PFC converter which provides regulated output voltage, input voltage clamped with voltage across switch. Also, buck topology provides short circuit protection and high efficiency within wide input range. However, the dead zone in input current is major problem in buck PFC topologies. This paper reviews the basic principles, various topologies and recent developments in control schemes to achieve high efficiency unity PF buck PFC converter for low power applications. Also, comparison is given between buck and boost converter. Based on literature review finally a conclusion is made with regards to given results.*

Key Words: *Boost, Buck, Buck-boost, PFC conversion, Unit PF, low THD, Buck topologies.*

1. INTRODUCTION:

Along with benefit of effective control over many applications power electronics converters have become the building block in various applications like SMPSs, UPS, integration of renewable energy resources with conventional systems and much more. Although with this easiness and control there comes power quality issues like voltage flicker, voltage distortion, harmonic current and of course poor power factor hence increasing the cost. Traditionally, diodes and thyristors perform the action of ac–dc conversion, providing controlled and semi controlled dc output with unidirectional and bidirectional power flow. Although, they hold the disadvantages of increasing the size of circuits, poor power quality injecting current harmonics, voltage distortion, low power factor at input ac mains with slow changing rippled dc output at load end. PFC converters provide fast dynamic response, reasonable power quality, high PF and output voltage. But as these converters are not ideal so power quality problems associated with these converters can be eliminated to a limit standardized by IEEE and IEC [1-3]. For low power and lightning application reasonable voltage regulation and high PF is required. This problem is overcome by using various active PFC controllers. The basic circuit of PFC converter is shown in figure.1 with help of this configuration unity PF and reasonable voltage regulation is achievable. This approach is called two stage approach, obviously the power stage goes through two conversion process which heavily penalize the efficiency and cost for low power application.

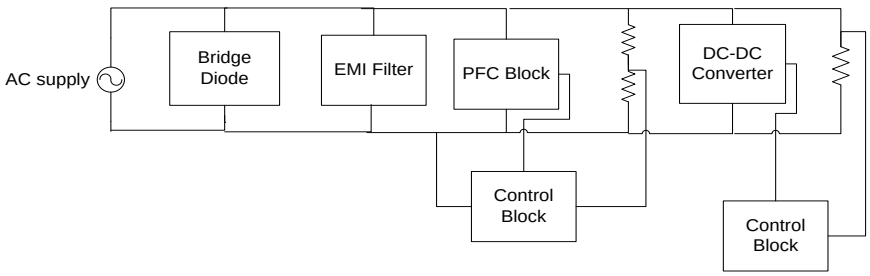


Figure. 1 basic PFC converter

However, these converters provide reasonable advantages in terms of the following reasons.

i. These converters guarantee the compliance of any regulation as they provide sinusoidal input line current.
ii. For universal line voltage it gives great performance.
iii. It provides variety of options to carry out both the isolation between line and load, and the hold-up time.
iv. The performance penalty due to the double-energy processing is partly mitigated by the reality that voltage is regulated on the storage capacitor.

Second stage design is possible as these topologies provide steady input voltage. Although attaining unity power factor is ideal aim, compliance with the regulations is not necessary. For instance, IEEE 519 and IEC 1000-3-2 equally accept the existence of harmonics in input current side [1-3]. This assumption has led to the publication in recent years of a significant number of papers, suggesting solutions that obtained many benefits over the two-stage technique.

2. STUDY OBJECTIVES:

This paper aims to categorize and compare numerous converters put forward by many authors for the ac–dc application with PFC and focusing the study in the low power range. Several techniques for PFC and THD harmonic elimination have been described and a few of them have obtained greater acceptance over the others.

3. METHODOLOGY:

Buck versus Boost PFC configuration:

The Comparison for Buck and Boost converter in terms of various parameters in given below. In terms of input current boost PFC converters have smooth and continues input current waveform. Conversely, input current for buck PFC is discontinues [4]. Thus, boost PFC can achieve high PF with lower THD. The inherent challenge for buck converter is continues and smooth current to attain low THD [5]. The output of boost PFC converter is more than the input voltage, though for many applications lower output is required, so additional stepdown regulation is needed after PFC [6]. In contrast buck converter has low output voltage so the switching losses will be less also lower voltage are better for device safety [6]. Compared to boost, buck topology is consistent and have higher efficiency at universal input because of less switching losses [6], [7], [8] [9]. In terms of design boost converter have low side switch which provides ease of implementation utilizing a low side gate driver circuit. Whereas, traditional buck topology utilizes a gate driver on high side, increasing the complexity of implementing techniques. Also, implementing input current control which is widely used for PFC control is achievable easier in boost converter than buck converter because of inductor placement [6].

Table 1. Comparison chart for Buck and Boost PFC converters

Parameters	Buck Topology	Boost Topology	Reference
Input characteristics	Discontinues input current, High THD.	Smooth and continues input current waveform, Low THD.	[4], [5].
Output characteristics	Low output voltage typically 80V which leads to low switching losses.	High output voltage leading typically 400V leading to high switching losses.	[6], [7],
Efficiency	High efficiency, consistent in full operation range	Low efficiency, because of high loses	[6], [7], [8], [9].
Design consideration	Complex design, challenging to implement control scheme for input current.	Easy design, easy to implement control scheme for input current	[6]

From the above factors, the boost converter is easier to achieve than buck PFC to implement, this open the door for various research techniques to simplify the control scheme and achieve high efficiency with unity PF.

Buck versus Buck-Boost topology for PFC conversion:

Buck-boost converters are available in non-isolated and isolated topology, other different configurations are buck-flyback, SEPIC, Zeta, Cuk. Furthermore buck-boost converter is classified as:

a) Unidirectional buck-boost topology

High frequency transformer isolation is provided to ensure suitable adaption of varying voltage applications. This topology is utilized in various applications like UPS source, BLDC motors, and battery charging circuits [10-15]. Furthermore, function suitability is provided with help of soft switching approach in high frequency switching applications, switching losses and stress is low in soft switching technique.

b) Bidirectional Buck-Boost Converters:

This topology is somehow relevant to matrix converter topology. This configuration can perform bidirectional power flow i.e. it can be used as either buck or boost mode. This topology can be used for high power application by replacing G.T.O with IGBTs and series diode usage can be excluded for reduced power loss and reverse voltage blocking

[16]. Though these configurations have good performance in high power application but these systems also have some drawbacks like more power losses because of high switching frequency, presence of two switches have more turn on and turn off losses, the soft switching technique increases the size and cost. Also, these converters when working in discontinues conduction mode (DCM) or Critical conduction mode (CRM) needs discontinuity in grid current thus they need a filter at input side to make current continues [8].

Advantages with Buck PFC converters:

Unidirectional Buck Converters: This topology consists of bridge diode step down DC-DC converter working as chopper, energy storage elements such as capacitor and inductor with filter elements. Numerous configurations are achievable for this kind of converters provide with isolated or non-isolated frequency transformer. Traditionally other isolated topologies are forward DC-DC, and half bridge. This configuration is a great choice to achieve high PF, low THD for AC input, less stress on components, lowered size of filter components, and fast response

Bidirectional Buck Converters: This topology utilizes devices like IGBTs, MOSFETs, and BJTs and a current source converter based on PWM technique with self-commutating elements. However, for high power application GTO is prefer over the others. The reverse blocking of voltage is accomplished with help of series diode. This topology brings advantages including reduced size of filter, safe working voltage for devices, and low THD. [17-22].

Along with providing safety to devices with low output voltage higher efficiency, and smaller reactive power buck PFC converter is good choice for low power application. But along with these advantages the only matter of concern with a buck PFC converter is a dead zone or cross over distortion problem in input current. A cross over distortion is a condition when input voltage drops below the boundary voltage, for this period the buck switch does not conducts current and hence a dead zone is generated causing harmonics and low PF. For a buck type topology voltage at output is set be fairly less than ac line voltage. Figure 2 illustrates current waveform with cross-over distortion at low input [23].

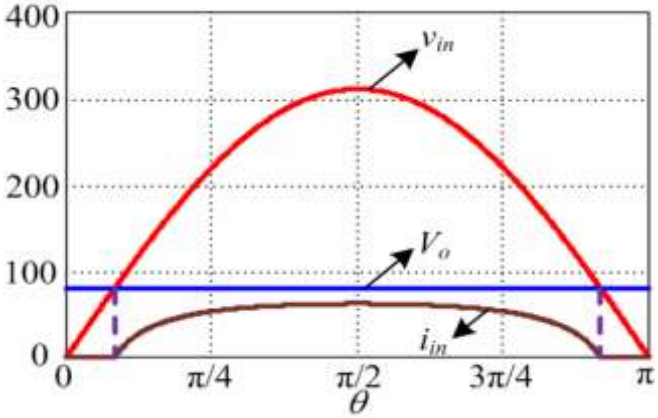


Figure 2. Conventional buck converter waveforms. Dead zone in input current (brown), Input voltage (red) and output voltage (blue)

This dead zone with conduction angle θ_c in radians is given as, [23]

$$\theta_{Cond} = 2\cos^{-1}\left(\frac{V_{out}}{V_{inp}}\right) \qquad (1)$$

here V_{out} and V_{inp} represent input and output voltage. From equation (1) it is clear that greater is output (V) lesser is conduction angle or in vice versa case lesser is input (V) higher is cross-over distortion or dead zone. [6]. The initial conduction angle is given as,[23]

$$\theta_1 = \sin^{-1}\left(\frac{V_o}{V_{in}}\right) \qquad (2)$$

ending at an angle

$$\theta_2 = \pi - \theta_1 \qquad (3)$$

The resultant total conduction angle for the buck converter can be quantified by,

$$\theta_c = \theta_2 - \theta_1 \qquad (4)$$

The input PF is directly affected by shapes formed by current waveform and the PF is defined as

$$PF = \frac{Active\ Power\ (P)}{Apperent\ Power\ (S)} \qquad (5)$$

Average active power is given in Watts and S is the apparent power in VA. With input sinusoidal peak voltage V_{in}, active power (P) is calculated as,

$$P = \frac{1}{\pi}\int_0^{\pi} Vin\ sin\,\theta\ i(\theta)\,d\theta \qquad (6)$$

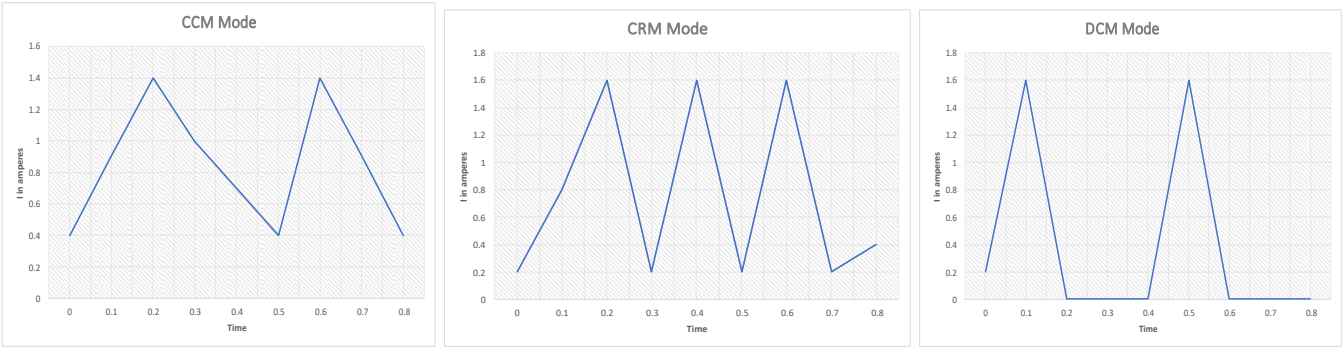
The $i(\theta)$ is average input current, as function of angle θ, the apparent power S is calculated as the product I_{rms} and V_{rms}, given as,

$$S = \frac{v_{in}}{\sqrt{2}} Irms \qquad (7)$$

For simplification, voltage ratio i.e. the ratio from output voltage V_o to peak input voltage V_{ip} is defined as

$$k = \frac{v_0}{v_p} \qquad (8)$$

The design approach of control scheme for a buck PFC is generally similar as for other PFC converters. The controller design comprises of two control loops one is called an outer loop and other known as inner loop [23]. The design of both control loop is very different from each other. The outer loop usually regulates the converter output voltage by controlling voltage. Conversely, the responsibility of inner loop is to make a desired shape the input current with help of current control technique. To ensure input current be pure sine wave the inner loop is design to give fast response while, to make sure the output to be not altered with output voltage ripple, the outer controller gives slower response. With a precise control a buck PFC can be operated in continuous conduction mode (CCM), critical conduction mode (CRM), or discontinuous conduction mode (DCM). Each technique has its own advantages or disadvantages. Techniques with CRM or DCM algorithm are more efficient than CCM, however it is very challenging to achieve simpler design for universal input range [6]. Hence, the precise, efficient and simple design for buck PFC is great challenge. Various researchers have done a plenty of research to overcome this problem, the detailed explanation, and comparison is given below.



Continuous Conduction Mode (CCM) | Critical Conduction Mode (CRM) | Discontinuous Conduction Mode (DCM)

4. ANALYSIS:

Buck PFC implementation techniques

Five implementation techniques are available for Buck PFC converter: traditional, bridgeless, inverted, interleaved, and pulse-assisting. A literature review for each implementation is briefly presented and explained.

a) **Conventional Buck PFC** In this technique the control is provided by connecting switch on high side as shown in Fig. 4. Study in [9] shows that a load dependent CCM or DCM operated buck with constant duty cycle can achieve a high PF (more than 0.9) with Discontinues Conduction Mode though lower PF (near 0.7) with Continues Conduction Mode [24].

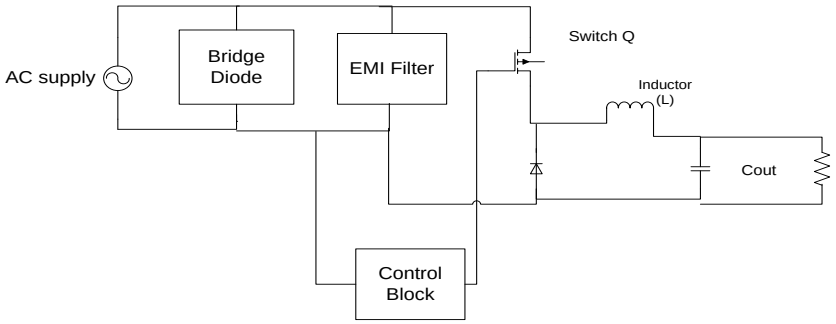


Figure 3. Traditional buck PFC topology.

The study in [8] consisting of a 100-watt buck PFC achieved zero voltage switching (ZVS) and high efficiency (over 96.5%) for a conventional buck PFC by utilizing variable switching mode CRM operated Constant on time control (COT) method, though the THD was high (up to 28.9%) without stating PF. The authors in [25] proposed variable duty cycle approach with fitting duty cycle method to achieve high input PF for DCM Buck PFC converter. The converter was operated in DCM mode which can achieve ZVS reducing the reverse recovery losses of diode and increase PF (up to 97%) though the control scheme contains more feedforward circuits increasing the complexity of circuit. Also study of [26], [27] is given in table (1).

b) Using switch on Low-Side or Inverted Configuration

Inverted Configuration utilizes buck switch with inductor on low side, as shown in fig.5. This configuration gives benefits of easy and robust design allowing usage of current sensor and gate driver switch on low side. However, the problem with this topology is complex circuitry, downstream sensing, common grounding issue and floating output voltage [6]. Various authors [6], [7], [9] have proposed many implementation techniques for low-side switch buck PFC converter. Study in [6] proposed a clamped-current buck PFC with current mode control operating in CCM. Study in [9] shows a higher efficiency can be achieved for inverted type buck topology as compared to clamped-current buck. An experimental setup with 100-watt prototype was presented which reduced switching losses, increasing efficiency up to 95.8% and a PF from 0.89 to 0.97 with low THD suitable for EN61000- 3-2 Class D application**.** [28] In this paper, a 50-W prototype CRM buck converter with tapped inductor is proposed converter operates with a maximum operational frequency as 70kHz. The soft switching operation is achieved by principle of resonance among the filter inductor and capacitor switch. The taping of inductor provides benefits of lower peak current which lowers switching and conduction loss. Also, the power stress on switch with CRM scheme is reduced. Th maximum achievable efficiency was given as about more than 96% without mentioning the THD. However, the circuit control scheme is complex and performance to achieve high efficiency at resonance frequency is more complex to design. Work in [29] proposed a single-stage UPF buck-boost converter to attain unit power factor with extended voltage conversion ratio capability. This topology provides many advantages which includes automatic PFC, less potential stress, zero-current turn-on, and low output ripple regulated voltage. However, this configuration put more current stress on power circuit elements, limiting the application of scheme up to only 150-W.

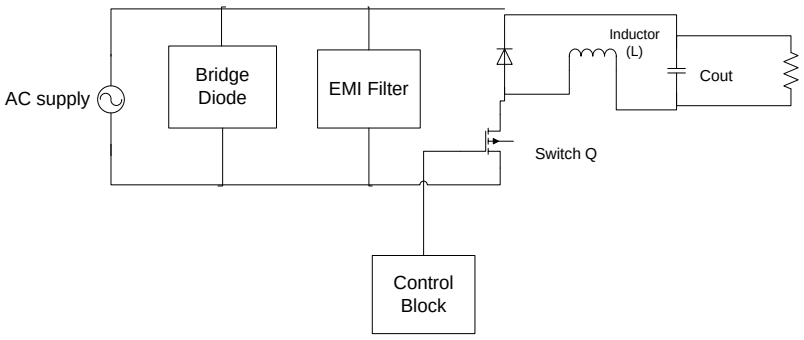


Figure 4. Inverted buck PFC topology.

The literature [30] proposed a 100-W prototype of constant on time CRM mode operated soft switching buck PFC topology. This topology achieved high efficiency and lower THD to meet IEC61000-3-2 class D applications. The efficiency achieved was 96.5% for universal input limits. However, this configuration requires large filter components because of discontinues input current and variable frequency.

c) Using Interleaved Buck PFC

A two parallel interleaved buck converters can improve performance and power capability as shown in fig. X. This topology provides benefits of halved input ripple current and doubling the ripple frequency providing usage of smaller size filters, these line filters yields in lower line current displacement factor hence improving the PF. [31], [32].

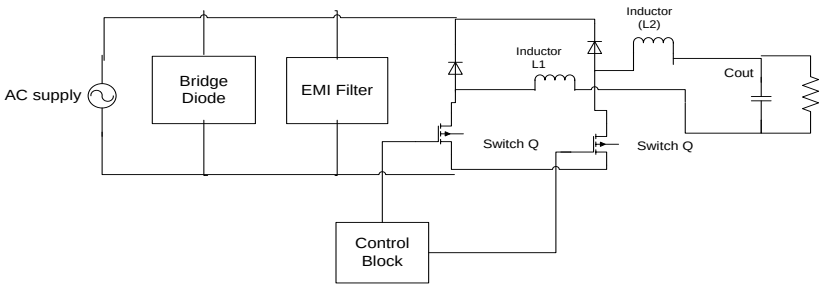


Figure 5. Dual inverted interleaved buck PFC topology

In [33], a high efficiency buck/buck-boost reconfigurable LED driver based on peak current control is presented. Research in [34] put forward an efficient COT scheme with optimal parameters. With a 100-W prototype a high PF with low harmonic is achieved passing the IEC-6100-3-2 class C limits for low power applications. The efficiency of proposed scheme is nearly 96% with input PF as 95.4%. Though the usage of two additional diodes, a floating driver circuit with a switch makes this configuration more complex and increasing the cost. The literature in [35] performed in depth performance comparison (consisting of efficiency, EMC and stress on electrical elements) in boost and buck type PFC under critical conduction mode (CRM). Results show that Buck PFC is 1% more efficient at low line input to its counterpart, also the experimental results confirmed that buck configuration is more suitable for low power application due to its low voltage swing. Research in [36] put forward a scheme to meet the IEC61000-3-2, Class C harmonics limits for lighting applications for the buck PFC converter for a front-end isolated high-brightness LED (HB-LED) application. For lightning applications, the lower harmonic order and regulated on time for switch was achieved by using a variable on-time controller with CRM mode critical conduction mode (CRM). The prototype of 150-W showed an efficiency of almost 96% for entire load line. However, for variable on time control more feedforward circuits is required which increases overall cost**.**

d) Buck PFC with Bridgeless topology

This topology eliminates usage of bridge diode for conversion and PFC application. This elimination increases efficiency as the diode switching losses are eliminated, the general configuration for bridgeless configuration is shown in figure 6. Many research attempts have been done to increase efficiency and high PF. [37], [38]

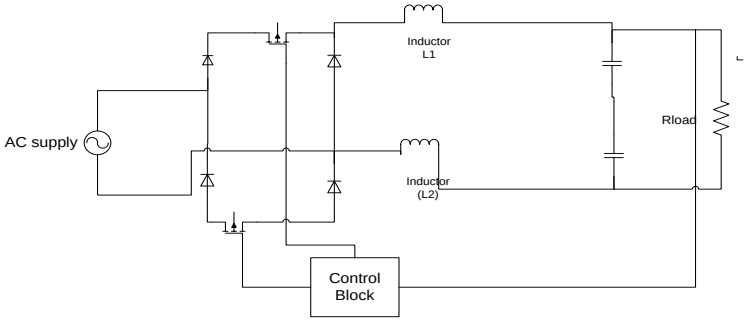


Figure 6. Bridgeless buck PFC topology.

Authors in [39] verified an experimental research work with a 700-Watt, 65kHz prototype, results show that efficiency is considerably improved at universal input range. An efficiency close to 96.4% was measured with 50% load where the line voltage ranges from 115 V to 230V. Bridgeless single inductor buck rectifier is presented in [40] that increases the efficiency of conventional buck power factor correction converters by reducing the number of simultaneously conducting semiconductor components. A PWM voltage control mode with output voltage sensor and error amplifier is utilized with PI controller and a total THD of 18.12% with input PF as 0.94 is obtained. Study in [41] presented an integrated buck–buck–boost (IBuBuBo) converter with no transformer. The experimental results show that it can achieve an efficiency of 89% and it can meet the IEC 61000-3-2 standards, the proposed topology was able to achieve the intermediate bus voltage up to 150V for any input or output condition.

e) Pulse-Assisting Buck (PAB) PFC configuration

The drawback of cross over distortion causing low PF and high THD can be significantly improved with the help of pulse assisting buck PFC topology. Authors in [42] presented a pulse assisting topology for a buck PFC converter, this topology utilizes additional switch and extra diode allowing current to pass when output voltage is higher than input voltage. Switch Q1 is utilized when the input voltage is higher than the output voltage the switch allowing current to flow in CCM mode. Conversely, switch Q2 is ON when input voltage is less than the input voltage allowing current to flow in DCM mode. With this topology the dead zone in current is effectively eliminated providing nearly a sinusoidal input current. Fig 9 exhibits current flowing in both different approaches. With an experimental results and prototype of 94-W efficiency over 96%, a high PF above 0.96 with low THD within IEC61000-3- 2 Class C standard is achieved.

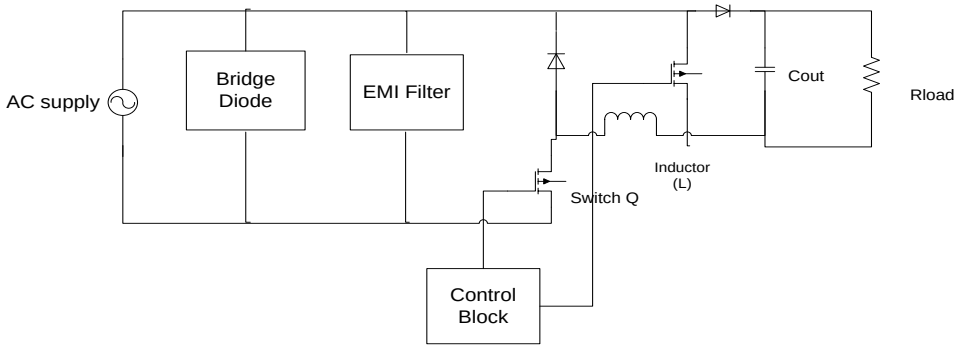


Figure 7. Buck PFC with Pulse-assisting topology.

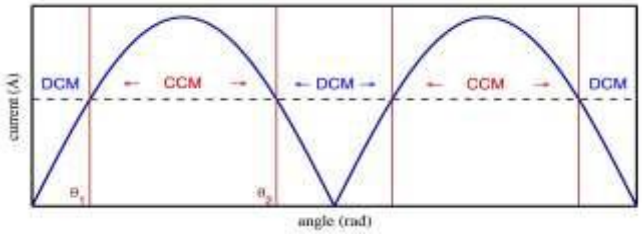


Figure 8. Current in CCM and DCM approach [10]

Authors in [43], [44], [45], proposed various control scheme using VOT and COT topologies to improve input PF of Buck converter. In [43], a new variable on time control mechanism is presented to increase the PF near to unity for a buck/ buck-boost converter operating in CRM mode for the low power application. Results show that almost unity PF can be achieved with low THD. However, this circuit arrangement needs more feed forward circuits to implement control strategy hence increasing the cost. Study in [44] proposed a CRM integrated buck-flyback topology to achieve high input PF. A variable on time scheme is proposed with help of input and output voltage to module the on time a high PF with low harmonics can be obtained. Almost, 95% efficiency is obtained but this configuration requires separate control feedforward circuits for buck and flyback switch and hence smooth transition is complex to achieve. Authors in [45] presented a UPC based control scheme for a boundary conduction mode (BCM) buck PFC converter. The authors also carried out comparison between UPC and Non UPC scheme in terms of output voltage ripple and losses, and results show that the input PF and efficiency of converter increased considerably and THD is in limit for low power usage. Authors in [46] proposed a non-isolated buck–flyback power factor (PF) correction (PFC) topology. This configuration provides grounding to both buck and flyback switch such that no floating driver circuit is required, results show that this topology is very effective for high power non isolated LED drive applications, However, one switch is required to be driven by a floating driving circuit, that increase the cost of topology.

5. RESULT:

Table (2) summarizes the research work of various authors with achieved efficiency, input PF over wide input range and rated load with different topologies and power ratings. Generally, a buck PFC topology is great choice for low power applications and exhibit great efficiency. PAB topology can achieve high input PF with Variable on time control scheme but this topology reduces efficiency. With Constant on time control both efficiency and high PF can be achieved but its design is still a big challenge. Also, the table and literature study show that for low power applications PAB, and inverted topologies exhibit good efficiency and can attain high PF. However, for higher applications interleaved topology can attain good efficiency and high PF. The bridgeless topology can also attain high efficiency at high power applications but this require precise design which is still a challenge.

Table 2. Various Buck PFC Topology Comparison Data

Buck Converter Topology	Power Ratting (W)	Control Strategy	Efficiency (%)	Input PF	Reference
Conventional	100		96.5-97.5	-	[8]
	-	VOT	96.4%	0.92-0.98	[25]
	100		78.6-80.8	0.97-0.99	[26]
	150		96.1-97.2	0.96	[27]
Inverted	90		96.1-96.8	0.89-0.97	[6]
	94	-	95.7-96.4	0.88-0.96	[7]
	100		95.8-97.0	0.89-0.97	[9]
	50	COT	96.6%	-	[28]
	150				[29]
	100	COT	96.5-97.2	0.82-0.98	[30]
Interleaved	300		96-97	0.95-0.98	[31]
	-		93-97	0.99	[32]
	100		96%	0.954	[34]
	150	-	96	-	[36]
Bridgeless	40		-	0.96	[37]
	700		94.6-95.2	0.89-0.95	[39]
	-	PWM control	-	0.94	[40]
	-	Transformer less	89%	-	[41]
Pulse-Assisting	94	-	93.1-96.2	0.94-0.99	[42]
	100	VOT	96.3	0.96-0.98	[43]
	100	VOT	95.3	0.965-0.985	[44]
	100	UPC VOT	95.8-97	0.96-0.986	[45]
	100	COT	94.5-95.8	0.94-0.97	[46]

6. CONCLUSION:

Active PFC is great choice to limit current harmonics, and power quality issues in low power applications. Boost PFC with AC/DC converter is generally used to attain high efficiency and high PF. However, this topology has various drawbacks which can be overcome by using a buck PFC topology with these converters. This paper reveals that a buck PFC is great choice for PFC application and this topology can achieve high PF by lowering the THD with great efficiency. For the sake of explanation, a limited example of medium and high-power applications with results is discussed and results show that the buck topology is well suited for lower power applications. The major challenge in a buck topology is a cross-over distortion or dead zone which appears when input is less than output. Various control techniques can be used to overcome this challenge variable on time control (VOT), constant on time control (COT) etc. With these control strategy various techniques are proposed that utilize basic configuration as discussed above i-e tadeonal, inverted, interleaved, bridgeless or PAB along with these configurations Continues conduction mode (CCM), Boundary conduction mode (BCM), or Discontinues conduction mode (DCM) to achieve pure input sinewave, higher efficiency and high PF with low THD. The literature shows that the traditional, inverted, and PAB topologies are greatly suitable with low-power applications. However, the interleaved and bridgeless topologies are among good choice for higher-power applications.

REFERENCES:

1. Limits for Harmonic Current Emissions (Equipment Input Current <16A per Phase), IEC 1000/3/2 Int. Std., 1995.
2. “Compliance testing to the IEC 1000-3-2 (EN 61000-3-2) and IEC 1000- 3-3 (EN 61000-3-3) standards,” Agilent, Tech. Rep. AN 1273, 2000.
3. “IEEE 519 Recommended practices and requirements for harmonic control in electrical power systems,” Tech. Rep., IEEE Industry Applications Soc./Power Engineering Soc., 1993.
4. S. Abdel-Rahman, “CCM PFC boost converter design,” Infineon, Tech. Rep. DN 2013-01, 2013.
5. “SMPS ac/dc reference design users guide,” Microchip, 2008, dS70320B.
6. B. Keogh, “Power factor correction using the buck topology—efficiency benefits and practical deisgn considerations,” Texas Instruments, Tech. Rep. SLUP264, 2010.
7. L. Huber, L. Gang, and M. Jovanovic, “Design-oriented analysis and performance evaluation of buck PFC front end,” IEEE Trans. Power Electron., vol. 25, no. 1, pp. 85–94, Jan. 2010.

8. J. Yang, J. Zhang, X. Wu, Z. Qian, and M. Xu, "Performance comparison between buck and boost CRM PFC converter," in Proc. IEEE Workshop Control Modeling Power Electron., June 2010, pp. 1–5.
9. H. Zeng and J. Zhang, "An improved control scheme for buck PFC converter for high efficiency adapter application," in Proc. IEEE Energy Conversion Congr. Expo., Sept. 2012, pp. 4569–4576.
10. D. H. Braun, T. P. Gihnore, and W. A. Maslowski, "Regenerative converter for PWM AC drives," in Industry Applications Society Annual Meeting, 1991., Conference Record of the 1991 IEEE, 1991, pp. 862-868 vol. 1.
11. D. M. Divan, G. Venkataramanan, and C. Chen, "A unity power factor forward converter," in Industry Applications Society Annual Meeting, 1992., Conference Record of the 1992 IEEE, 1992, pp. 666-672 vol. 1.
12. S. Funabiki, N. Toita, and A. Mechi, "A single-phase PWM AC to DC converter with a step up/down voltage and sinusoidal source current," in Industry Applications Society Annual Meeting, 1991., Conference Record of the 1991 IEEE, 1991, pp. 1017-1022 vol 1.
13. R. Hoh and K. Ishizaka, "Single-phase sinusoidal rectifier with step-up/down characteristics," Electric Power Applications, IEE Proceedings B, vol. 138, pp. 338-344, 1991.
14. M. H. Kheraluwala and R. W. De Doncker, "Single phase unity power factor control for dual active bridge converter," in Industry Applications Society Annual Meeting, 1993., Conference Record of the 1993 IEEE, 1993, pp. 909-916 vol.2.
15. J. Sebastian, J. Uceda, J. A. Cobos, J. Arau, and F. Aldana, "Improving power factor correction in distributed power supply systems using PWM and ZCS-QR SEPIC topologies," in Power Electronics Specialists Conference, 1991. PESC '91 Record., 22nd Annual IEEE, 1991, pp. 780-79l.
16. H.-L. Cheng, Y-C. Hsieh, and C.-S. Lin, "A novel single-stage high-power-factor ACIDC converter featuring high circuit efficiency," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 524-532,2011. [41] K. M. Bogdan and T. Citko, "Application of the AC link in power con-version systems," in Proc. EPE'97, 1997, pp. 4.459-4.464.
17. M. Brkovic and S. Cuk, "A novel single stage AC-to-DC full-bridge converter with magnetic amplifiers for input current shaping," in Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE, 1995, pp. 990-995 vol.2.
18. D. Casini and G. Marola, "A quasi optimal technique for the on-line control of ACIDC and DC/AC PWM converters," in Industrial Electronics, Control and Instrumentation, 1994. IECON '94., 20th International Conference on, 1994, pp. 97-101 vol 1.
19. L. C. de Freitas, A. A. Pereira, and J. L. Andres, "A high power factor operating self-resonant-PWM forward converter," in Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual, 1995, pp. 440-446 vol. 1.
20. M. C. Ghanem, K. AI-Haddad, and G. Roy, "Soft commutated unity power factor boost assisted parallel resonant converter (UPFBPRC)," in Industrial Electronics, Control, and Instrumentation, 1995., Proceedings of the 1995 IEEE IECON 21st International Conference on, 1995, pp. 265-270 vol 1.
21. A. A. Pereira, J. B. Vieira, Jr., and L. C. de Freitas, "A lossless switching forward converter with unity power factor operation," in Industrial Electronics, Control, and Instrumentation, 1995., Proceedings of the 1995 IEEE IECON 21st International Conference on, 1995, pp. 329-334 vol. 1.
22. S. A. Streng and R. J. King, "Ripple feedback for the resonant-filter unity-power-factor rectifier," Power Electronics, IEEE Transactions on, vol. 7, pp. 453-461, 1992.
23. Comparison of Input Power Factor Correction Techniques for Buck Converters in Single-Phase Wireless Power Transfer Systems Hyeun-Tae Cho, Jingook Kim, Jeehoon Jung and Katherine A. Kim School of Electrical and Computer Engineering Ulsan National Institute of Science and Technology Ulsan, Kore 978-1-4799-6610-3/15/$31.00 c 2015 IEEE
24. H. Endo, T. Yamashita, and T. Sugiura, "A high-power-factor buck converter," in Proc. IEEE Power Electron. Specialists Conf., vol. 2, June 1992, pp. 1071–1076.
25. Memon, A.H., Nizamani, M.O., Memon, A.A., Memon, Z.A. & Soomro, A.M. (2019). Achieving high input power factor for DCM Buck PFC converter by variable Duty-Cycle Control. 3C Tecnología. Glosas de innovación aplicadas a la pyme. Speciaal Issue, November 2,
26. V. Grigore and J. Kyyra, "High power factor rectifier based on buck converter operating in discontinuous capacitor voltage mode," IEEE Trans. Power Electron., vol. 15, no. 6, pp. 1241–1249, Nov. 2000
27. J. Yang, X. Wu, J. Zhang, and Z. Qian, "Variable on-time controlled ZVS buck PFC converter for HB-LED application," in Proc. IEEE Applied Power Electron. Conf., Mar. 2011, pp. 65–70.
28. The Zero Voltage Switching (ZVS) Critical Conduction Mode (CRM) Buck Converter With Tapped-Inductor Jong-Hu Park, Student Member, IEEE, and Bo-Hyung Cho, Senior Member, IEEE. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 20, NO. 4, JULY 2005.

29. Buck–Boost-Type Unity Power Factor Rectifier with Extended Voltage Conversion Ratio Esam H. Ismail, Member, IEEE, Ahmad J. Sabzali, Member, IEEE, and Mustafa A. Al-Saffar, Member, IEEE. IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 55, NO. 3, MARCH 2008.
30. B. Keogh, G. Young, H. Wegner, and C. Gillmor, "Design considerations for high efficiency buck PFC with half-bridge regulation stage," in Proc. IEEE Applied Power Electron. Conf., Feb. 2010, pp. 1384–1391.
31. Design Considerations of Soft-Switched Buck PFC Converter With Constant On-Time (COT) Control Xinke Wu, Member, IEEE, Jianyou Yang, Junming Zhang, Member, IEEE, and Ming Xu, Senior Member, IEEE IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 26, NO. 11, NOVEMBER 2011
32. H. Choi, "Design and analysis of an interleaved boundary conduction mode (BCM) buck pfc converter," J. Power Electronics, vol. 14, no. 4, pp. 641–648, July 2014. [13] V. F. Pires and J. F. Silva, "Single-stage double-buck topologies with high power factor," J. Power Electronics, vol. 11, no. 5, pp. 655–661, Sept. 2011
33. Cho, Kunhee, and Ranjit Gharpurey. "An Efficient Buck/Buck-Boost Reconfigurable LED Driver Employing
34. Xie, X., Zhao, C., Zheng, L., & Liu, S. (2012). An improved buck PFC converter with high power factor. IEEE Transactions on power electronics, 28(5), 2277-2284
35. Performance Comparison between Buck and Boost CRM PFC Converter Jianyou Yang, Junming Zhang, Xinke Wu, and Zhaoming Qian College of Electrical Engineering, Zhejiang University Hangzhou, China IEEE
36. Variable On-Time (VOT)-Controlled Critical Conduction Mode Buck PFC Converter for High-Input AC/DC HB-LED Lighting Applications Xinke Wu, Member, IEEE, Jianyou Yang, Junming Zhang, Member, IEEE, and Zhaoming Qian, Senior Member, IEEE. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 27, NO. 11, NOVEMBER 2012.
37. A. Emrani, M. Mahdavi, and E. Adib, "Soft switching bridgeless pfc buck converters," J. Power Electronics, vol. 12, no. 2, pp. 268–275, Mar. 2012.
38. L. Huber, L. Gang, and M. M. Jovanovic, "Design-Oriented analysis and performance evaluation of buck PFC front-end," IEEE Trans. Power Electron., vol. 25, no. 1, pp. 85–94, Jan. 2010
39. Y. Jang and M. Jovanovic, "Bridgeless buck PFC rectifier," in Proc. IEEE App. Power Electron. Conf., Feb. 2010, pp. 2329.
40. "Modified Bridgeless Buck Rectifier with Single Inductor for Power Factor Correction" Shabana J SSRG International Journal of Electrical and Electronics Engineering (SSRG-IJEEE) – Volume 4 Issue 4 – April 2017.
41. A High Step-Down Transformer Less Single-Stage Single-Switch AC/DC Converter Shu-Kong Ki, Student Member, IEEE, and Dylan Dah-Chuan Lu, Senior Member, IEEE. IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 28, NO. 1, JANUARY 2013.
42. J. Xu, M. Zhu, and S. Yao, "Distortion elimination for buck pfc converter with power factor improvement," J. Power Electronics, vol. 15, no. 1, pp. 10–17, Jan. 2015.
43. Memon, A. H., Baloach, M. H., Sahito, A. A., Soomro, A. M., & Memon, Z. A. (2018). Achieving High Input PF for CRM Buck-Buck/Boost PFC Converter. IEEE Access, 6, 79082-79093.
44. Memon, A. H., Yao, K., Chen, Q., Guo, J., & Hu, W. (2016). Variable-on-time control to achieve high input power factor for a CRM-integrated buck–flyback PFC converter. IEEE Transactions on Power Electronics, 32(7), 5312-5322.
45. Memon, A. H., & Yao, K. (2018). UPC strategy and implementation for buck–buck/boost PF correction converter. IET Power Electronics, 11(5), 884-894.
46. A Novel Integrated Buck–Flyback Nonisolated PFC Converter With High Power Factor Xiaogao Xie, Member, IEEE, Chen Zhao, Member, IEEE, Qiang Lu, Member, IEEE, and Shirong Liu. IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 60, NO. 12, DECEMBER 2013