Implementation of Phase Disposition Multicarrier Pulse Width Modulation Technique for Symmetrical Developed H-Bridge Multilevel Inverter

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Abstract: *These days multilevel inverters are widely used in high power and medium voltage applications due to their advantages, such as lower switching losses, lower voltage stress on solid state devices and lower harmonic distortion in the output voltage than the two-level converters. In this paper, 5-level symmetrical developed h-bridge multilevel inverter with two symmetric DC sources has been performed successfully and its performance is investigated in MATLAB software. Recently, different modulation methods used for the operation of multilevel inverters. A phase disposition multicarrier pulse width modulation (PD-MCPWM) is used in this paper to reduce the THD which is 26.18% in the MLI output voltage.*

Key Words: *Developed H-Bridge, Multilevel Inverter, Multicarrier PWM technique, Phase Disposition(PD), Total Harmonic Distortion.*

1. INTRODUCTION:

Multilevel inverters are widely used in moderate to high power applications, like alternative energy sources, industrial equipment, HVDC, adjustable frequency controllers, wireless power transfer, flexible ac transmission system FACTs controllers etc [1]. Today, the progression in the generation and use of renewable energy sources has modified the power system. With this rapidly develop technology, the need and requirement for efficient conversion of power from DC to AC are achieved economically through the use of an inverter [2-4]. The conventional inverters generate square waves or quasi waves, they cannot generate pure sinusoidal waves. The output contains harmonics which makes conventional inverter least efficient and often switching losses and leads to various power quality problems [5-7]. To overcome these incompetent factors of the two-level inverter, the MLI is preferable in high power applications [8]. Multi-level inverters produce more levels than 2-level inverters at the output. The output waveform is nearly similar to sinusoidal shape, reduces THD, lower dv/dt per switching and lower electromagnetic interference. Flying capacitor, diode-clamped and cascaded H-bridge multilevel inverters are conventional inverters [9]. The Cascade H bridge is more economical and efficient and generates the output voltage levels with less devices compared to flying capacitor and diode clamped MLIs [10-11]. MLI is further classified into symmetrical and asymmetrical inverters on the basis of voltage magnitudes. In symmetric, all sources have the same level of magnitude, while asymmetric inverters are those that have a different source voltage magnitude [12-18]. Recently, attention is paid to increase output voltage levels of multilevel inverters with less components. These inverters are referred as reduce device count multilevel inverters.

The developed h-bridge MLI is a modified version of cascaded H bridge inverter which generates more levels with small number of devices. The increased levels are made with several control techniques. Multicarrier PWM control (MCPWM) techniques are widely used in MLIs. Phase shifted and level shifted modulations are the types of MCPWM. Total harmonic distortion THD ratio is eminent in phase shifted then in level shifted modulation [19-20]. The level shifted multicarrier PWM further classified into phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD). The carriers of PD are same in amplitude, frequency and phase. In APOD technique, the carriers above and below zero reference are 180 degrees out of phase with their neighboring carriers, while in POD all carriers are 180 degrees phase shifted from their adjacent carriers [21-22]. Multicarrier techniques are classified as shown in Fig. 01. Application of PWM control algorithm is mainly depend on the higher and lower switching frequencies (mega Hz - few or hundred Hz). [23-25].

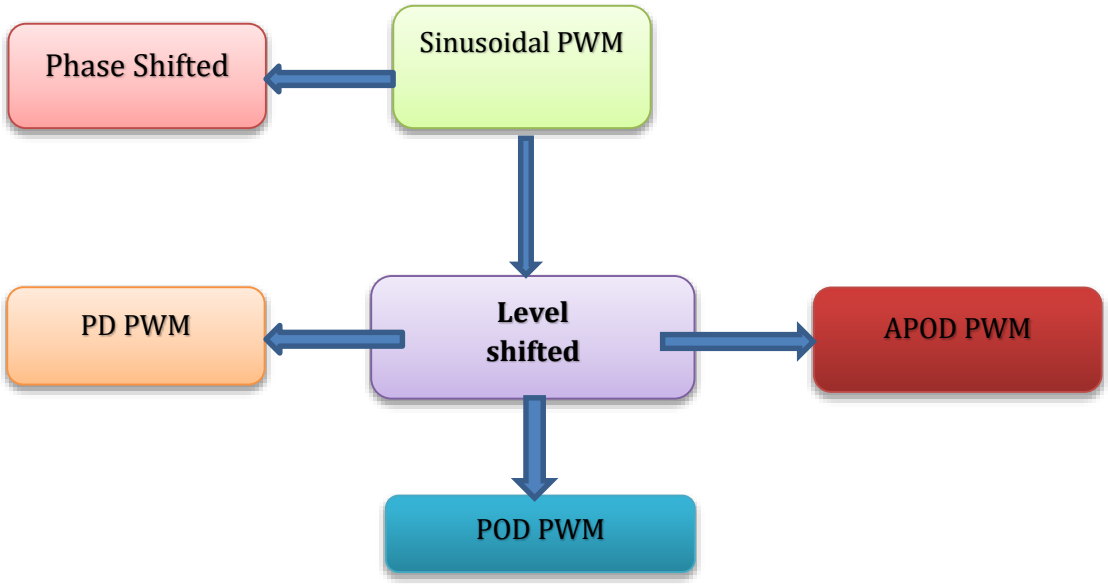


Fig. 01. Classification of Modulation Technique

2. METHODOLOGY:

Developed H bridge multilevel inverter

The circuit diagram of five-level developed h-bridge MLI is presented in fig. 02. It consists of two symmetrical 24 V DC sources and six solid state devices [22]. It generates positive, negative and zero levels. All of these switching operation levels are represented in Table 1, where switching status 0 indicates off and 1 indicates switching on of the switching devices. Number of levels in output voltage, switches, dc sources and maximum output voltage are obtained by Eq. (1), Eq. (2), Eq. (3) and Eq.(4) respectively. The 'n' in these equations indicate the number of dc sources in each leg of the MLI.

$$N_{level} = 2^{2n+1} \quad (i)$$

$$N_{sw} = 4n + 2 \quad (ii)$$

$$N_{source} = 2n \quad (iii)$$

$$V_o = V_1 + V_2 \quad (iv)$$

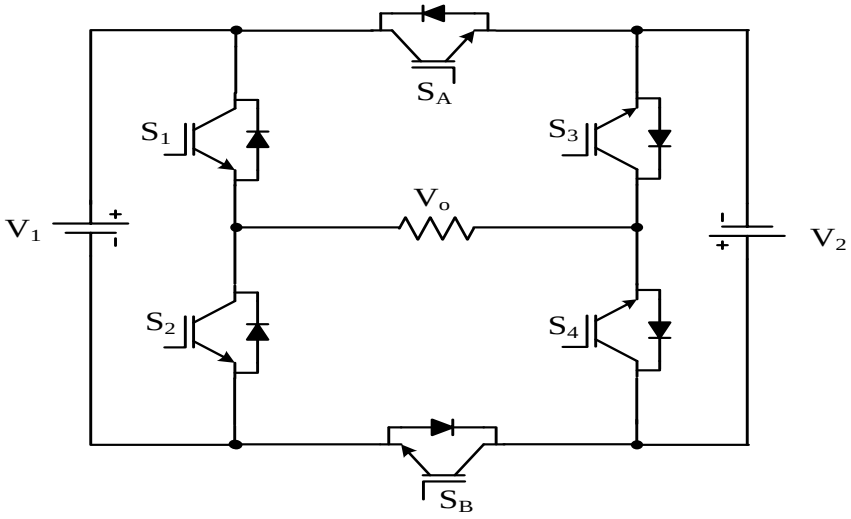
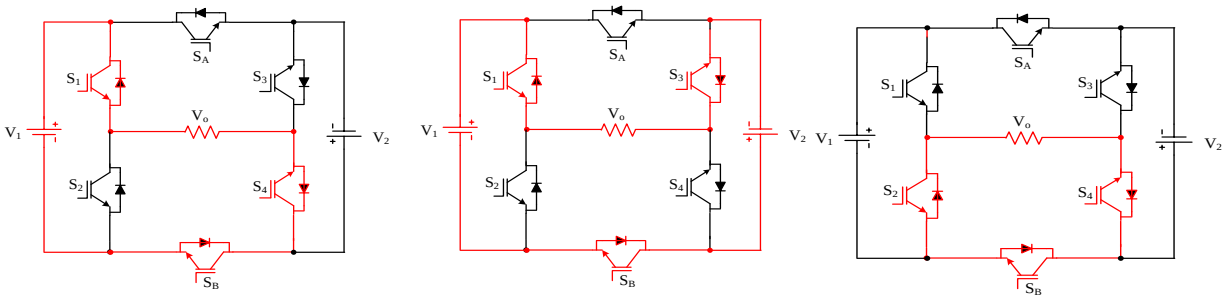


Fig. 02. Five level developed h-bridge MLI

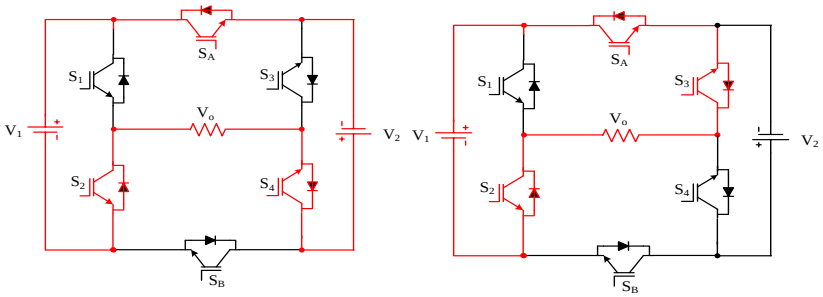
TABLE I SWITCHING OPERATION

Modes	S1	S2	S3	S4	Sa	Sb	Vo
1	1	0	0	1	0	1	V1
2	1	0	1	0	0	1	V1+V2
3	0	1	0	1	0	1	0
4	0	1	0	1	1	0	-(V1+V2)
5	0	1	1	0	1	0	-V1

The switching operation of symmetrical developed H-Bridge multilevel inverter is demonstrating the Individual switching modes of the proposed topology. These modes are illustrated in Fig. 3. As seen in mode 1, the output through the load will be **V1** when switches **S1, S4,** and **Sb** will remain close, during this cycle the other remaining switches will turn off; in mode 2, the output through the load will be **V1 + V2** when switches **S1, S3** and **Sb** remain turn on and during this period other switches will turn off; in mode 3, the output through the load will be **zero** when **S2, S4** and **Sb** remain close; the output through the load will be **-(V1+V2)** when switches **S2, S4** and **Sa** remain close during this time other remaining switches will turn off as shown in mode 4. And finally, when switches **S2, S3** and **Sa** remain closed, then the output through the load will be **-V** as shown in mode 5.



(Mode 1) V1 (Mode 2) V1+V2 (Mode 3) 0



(Mode 4) – (V1+V2) (Mode 5) - V1

Fig. 03. Switching modes from Mode 1 to Mode 5

Simulation model of developed H bridge multilevel inverter

In this paper, the simulation model for symmetrical developed cascaded H bridge is developed in MATLAB software. Fig.4 presents the simulation model of MLI. A phase disposition PWM multicarrier technique is implemented to minimize the (power) harmonics of MLI. This technique is shown in Fig.5 which comprises a reference signal with a triangular wave carriers. Each carrier is in phase and level shifted. The resulting signals alter the position at each crossing point of the reference wave and the carrier. In this strategy, the reference signal is continually related to each triangular carrier. In this technique, when triangular carrier is smaller than the reference wave, the output will be 1 and when the triangular carrier is larger than the reference, the output will change position.

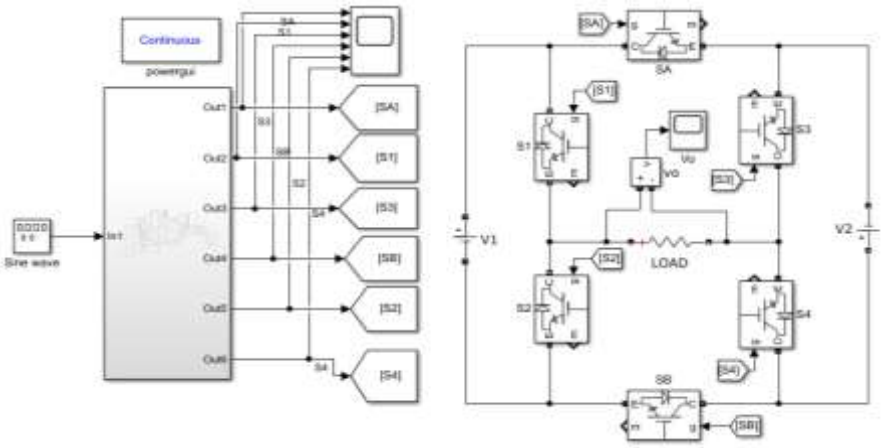


Fig.4 Simulation Model for 5-level Symmetrical Developed MLI

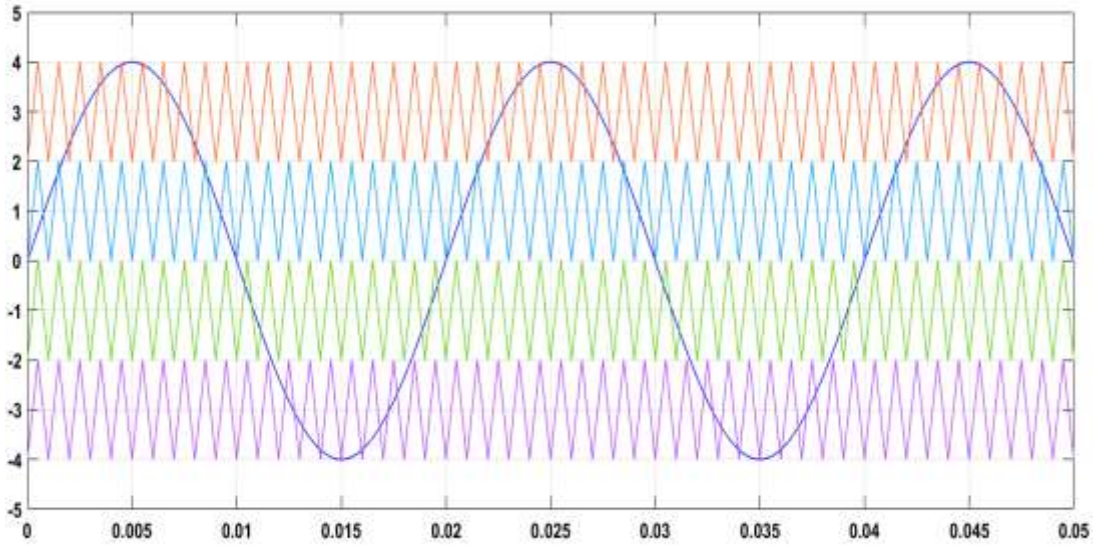


Fig. 5 waveform of *Phase Disposition Multicarrier PWM technique*

3. RESULT:

The multilevel inverter is simulated with the parameters as given in Table 01. A Phase disposition PWM multicarrier technique is used to produce switching pulses for IGBT connected in MLI. The switching signals are shown in Fig. 06. The five level output voltage waveform of MLI is illustrated in Fig. 07. For power electronic converters, THD is an important parameter, that measures the level of the harmonic components in the waveform. The harmonics of the waveform of the output voltage of the developed h-bridge MLI is illustrated in Fig.8. From the harmonic spectrum it is observed that when implementing the phase disposition multicarrier technique, the THD of developed h-bridge MLI is 26.18 %. This value can be further reduced by increasing the levels in output voltage.

Table 02: Parameters of simulation MODEL

Model Parameters	
No. of Switches	6
No. of DC Sources	2
Sine wava frequency	50 Hz
Switching frequency	1000 Hz
Resistive load	10 Ω
Output Voltage levels	5
Magnitude of DC sources	24 V

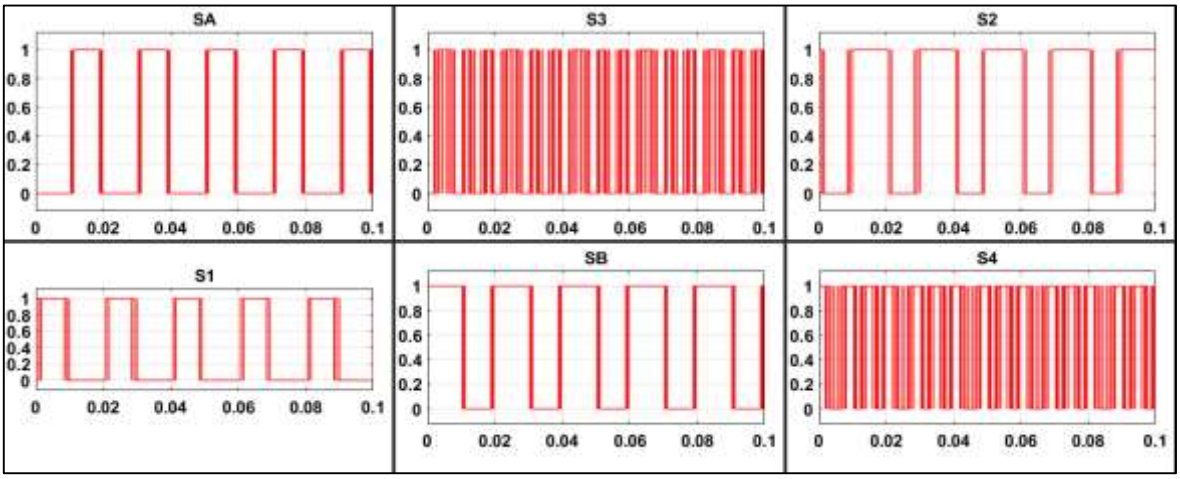


Fig. 06. PWM Signal to trigger switches from s1 to s5

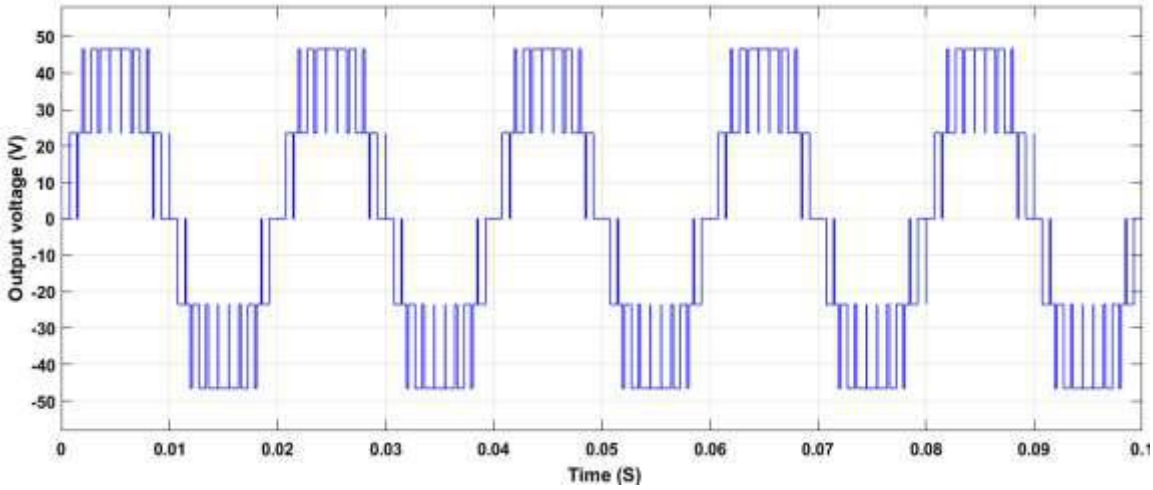


Fig. 07. Five- level output Voltage Waveform

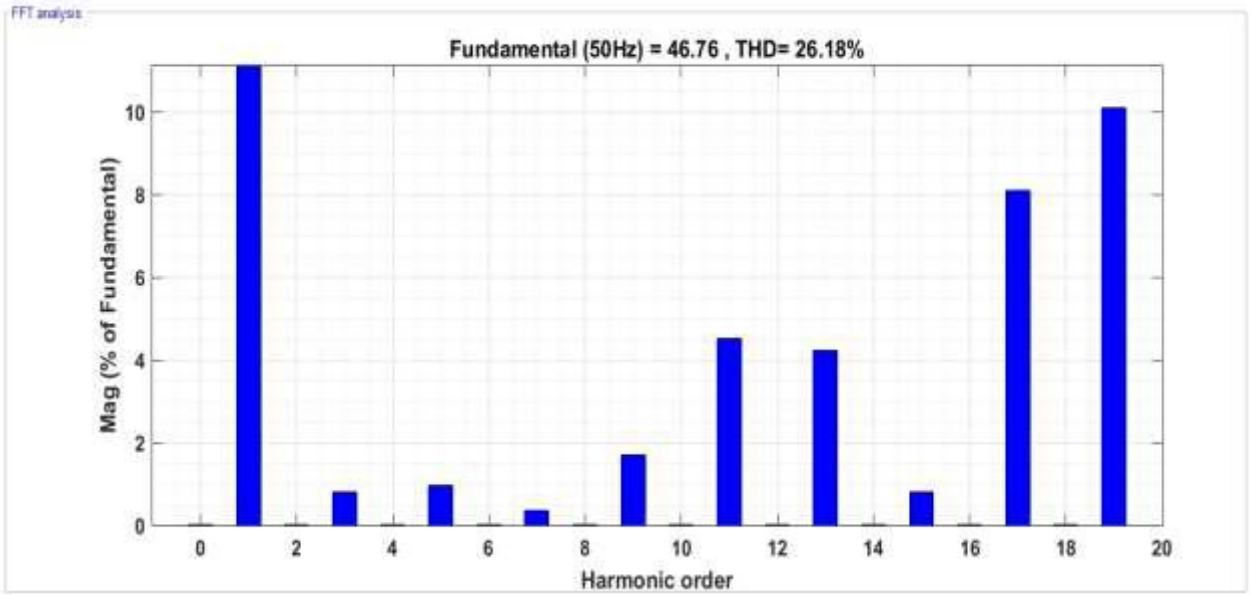


Fig. 08. Harmonic spectrum of Output Voltage

4. CONCLUSION AND FUTURE RECOMENDATIONS:

Advanced developed MLI topography have been evolving for additional benefits along with lower expenditure, optimum size, lower volume, lower losses, and high reliability. Multilevel inverter configuration for a number of major requirements are emerging as a versatile candidate for the energy sector. With the fast development of power electronic engineering science, several MLI topography were constructed by the articles using with reduced number of solid state

device. Just currently a range of multilevel inverter anatomy with reduced number of solid state device are built for various purposes such as engine drives, implementation of sustainable energy grids, FACTs, electricity extraction, etc. Hence, in this paper, the performance of a developed h-bridge topology is investigated in symmetrical mode. The simulated model is successfully developed in MATLAB software. A phase disposition multicarrier PWM technique is implemented in MLI to minimize the harmonics. It is concluded from the results that the total harmonic distortion in the output voltage is 26.18 %. By increasing the levels in output voltage of developed h-bridge, the THD value can be further reduced.

Current and prospective MLI topography with reduced number of solid state device models need to address a number of problems like portable MLI-based module configuration, frustration tool, large potential surges, radiant pressure, and system failure. In regards to model dimension, continual initiatives are also rendered to perform numerous MLI configuration appropriately i.e. Physical problems including regulating the DC-connection potential, malfunction drive through electricity, energy uncoupling, THD command as well as manipulate of energy efficiency. Picking up conventional MLI anatomy onto account, to the highest degree latest study of articles suggests the solutions to real problems. Another of the new developments in such a sector can be the deployment of wide band-gap devices in MLI topologies with reduced solid state device. That would introduce collectively a lot of benefits. For example, Silicon control component ' large-temperature ability are utilized to reduce warming circuits, simultaneously enhancing energy efficiency. And also the prospect to reduce the ride footprint as well as its costs related via boosting the energy output. With the implementation of Silicon control component an incorporated rotor drive could be achievable in the forthcoming days for reasonable and large-power requirements. In this kind of situation, the latest MLI with reduced number of solid state device usage structure for drives would proceeds into consideration concerns like rapid breakdown of the rotor axle, consistency, diminution of outflow current as well as removal of CMV. Furthermore, the introduction of alternative energy into the electricity network via the correct MLIs slowly pushes grid and utility towards the prospective power system. Furthermore, the introduction of alternative resources into the power system network via the correct MLIs slowly pushes grid and distributed network towards the prospective smart power system. It may face huge problems and situation to design configuration and govern of MLI with reduced number of solid state device. In this kind of case many network code specifications being established to preserve the desired power. To meet these requirements and fundamental problems, like peak power production, unstable current injecting into the system and outflow current, a number of articles are required to carry out. Ultimately, worries are continually raised related with optimal usage of electric power, enhance the efficiency of energy, reducing pollution etc. Because of this, advancements are already taking place in MLI with reduced number of solid state device, and are predicted to increase.

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